# MosfetModel: Modeling and characterization of n-MOSFETs

A. Bsiesy,
Inter-university Center for Micro-Electronics (CIME)

## Day 1: Process and device simulation

Due to the steady increase in the complexity of the electronic circuits, design and simulation activities gained a strategic role in the integrated circuit manufacturing industry. Indeed, simulation allows a remarkable gain of time in the design, optimization and processing of electronic devices. The aim of this practical course is to give an overview of the different tools currently used for process and device simulation in a large variety of semiconductor technology including the MOS application. Indeed, bipolar, optoelectronic, SOI (Silicon On Insulator) as well as TFT (Thin Film Transistor) technologies are supported by these simulation tools. The simulation platform used in this course is provided by *Silvaco International.* It includes state of the art 2D process simulation tool "Athena" and a 2D advanced device simulation tool "Atlas".

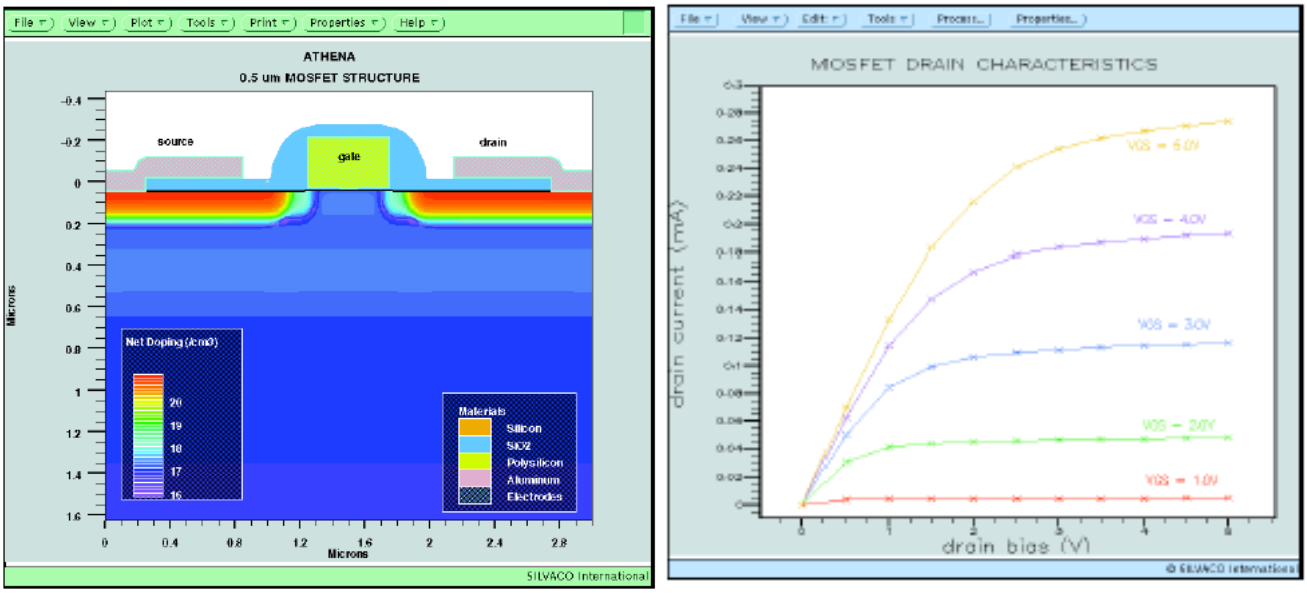


Figure 1, left : Two-dimensional 0,5um MOSFET structure with spacers simulated by Athena showing doping contours and the different materials. Right: Different MOSFET Id-Vd curves at different gate voltages simulated by Atlas.

The introduction section will recall the simulation hierarchy scheme which gives an overview of the design flow of an integrated circuit. The simulation methodology will then be presented; starting from physical models that leads to the coupled Poisson and transport partial differential equations (PDEs), followed by discretization techniques of the PDEs and ending by the numerical methods (Newton, Gummel, Block) of obtaining solutions.

Simple examples of process and device simulation will then be run in order to get started with the simulation tools. The MOSFET structure will be generated by Athena using fabrication process simulation. Physical parameters will be extracted including sheet resistance, oxide thickness, doping …. Electrical simulation will then be performed and compared to the device test results. Any deviation from the experimental results involving for example the threshold voltage, carrier mobility…will be discussed in the light of process experimental conditions.

Some typical examples of simulation of the MOS advanced features involving the “short channel” effects and the quantum effects will be analysed.

Fig. 2 : Mosfet characterization practical at ESONN 2004.

**Day 2: Electrical characterization of integrated semiconductor devices**

Device-level electrical test is a fundamental tool used for in-line and off-line monitoring of the integrated circuits manufacturing as well as in the research field on advanced integrated electronic devices. The main goal of this practical course is to get familiarized with the electrical test instrumental environment and with the test methodology of some of the main integrated devices, namely, the MOS capacitor, the diffused resistor, the n-type MOS field effect transistor (n-MOSFET) and the p-n diode. These tests will be conducted on the devices fabricated during a clean room practical course by another group of ESONN students. This makes possible a feedback on the fabrication process that usually reveals the impact of the process on the electrical characteristics.

More precisely, this course will show how physical (oxide thickness, doping…) as well as electrical parameters (threshold voltage, carrier mobility…) can be extracted from the device electrical characterization. Basic physical and electrical models will be applied to the analysis of the device characteristics. The behaviour of MOS capacitors in equilibrium, accumulation, depletion, and inversion regions will be examined. We will examine the capacitance-voltage characteristics of MOS capacitors from accumulation region to depletion region and study the effect of interfacial oxide charges on the MOS capacitor C-V characteristics. The n-MOSFET current-voltage characteristics will then be analysed in different bias conditions. Low-field carrier mobility in the inversion channel will be extracted using “long-channel” MOSFET models, and compared to the bulk value. The mobility roll-off observed at high electric field will then be characterized and modelled. The n-MOSFET sub-threshold current will be analysed in the light of the device electrical properties, in particular the density of surface states at the silicon-dielectric interface that can be extracted from the MOS capacitor analysis. It will be shown how this “leakage current” is detrimental for the static power consumption in the integrated circuits. Some short-channel effects in the MOSFET will then be pointed out such as the threshold voltage roll-off and current leakage. This will show why special measures must be taken to prevent these short-channel effects namely by following some "scaling rules" while scaling down MOSFETs geometry.